Amendments to the Drawings:

The attached replacement drawing sheets include changes to FIGS. 6, 7A, 7B, 8A and 8B to indicate that they show prior art.

REMARKS

Claim Status

Claims 1, 2 and 5 are presented for examination, with claims 1 and 5 being independent claims. Claims 3, 4, 6 and 7 have been withdrawn from consideration. The drawings have been amended. Claims 1, 2 and 5 have been amended. No new matter has been added by way of the above amendments. Reconsideration of the application, as amended, is respectfully requested.

Overview of the Office Action

The drawings were objected to by the Examiner. Withdrawal of this objection is requested.

Claims 1, 2 and 5 have been objected to based on certain informalities. Withdrawal of this objection is in order, as explained below.

Claims 1, 2 and 5 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,823,501 ("*Dahl*"). Applicants have carefully considered the Examiner's rejections and the comments provided in support thereof. For the following reasons, Applicants respectfully assert that all claims presented for examination in the present application are patentable over the cited reference.

Amendments Addressing Objections and Formalities

The drawings have been objected to because Figs. 6, 7A, 7B, 8A and 8B should be designated by a legend such as --Prior Art--. In response to this objection, Applicants have amended the drawings in a self-explanatory manner. Reconsideration and withdrawal of the objections to the drawings are respectfully requested.

Claims 1 and 5 were objected to because "'the measurement' (line 6) should be --each--...; 'which' (line 7) should be --said wiring line--". In claim 2, "'which the' (line 3) should be --which each--". In response to these objections, claims 1, 2 and 5 have been amended in a self-explanatory manner. Withdrawal of these objections is, therefore, in order.

Descriptive Summary of the Prior Art

Dahl discloses "methods for generating a padring layout design". *Dahl* (Abstract, lines 2-3) states, "these methods utilize automation while still allowing customization". *Dahl* (Abstract, lines 7-10) teaches that the padring is broken down into zones in which slots having bumps/bond pads areas, I/O cell areas, and/or edge logic cell areas are laid out in a regular pattern through an instantiation process. Finally, *Dahl* (Abstract, lines 13-18) teaches that the bumps/bond pads, I/O cells, and edge logic cells are laid out in respective bumps/bond pads areas, I/O cell areas, and/or edge logic cell areas according to algorithms associated with the patterns and using a variety of maps which associate a logical netlist with a physical layout design.

Summary of Subject Matter Disclosed in the Specification

The following descriptive details are based on the specification. They are provided only for the convenience of the Examiner as part of the discussion presented herein, and are not intended to argue limitations which are unclaimed.

A semiconductor device design method and design program are disclosed for automatically determining layout of a semiconductor device which has measurement terminals for measuring voltage, logic state, or the like, on wiring lines which connect the circuit blocks (see pg. 4, lines 14-18 of the originally-filed specification).

The design method comprises the steps of:

(i) registering measurement terminals as cells in design rules, together with the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device, and each measurement terminal is connectable to a wiring line for connecting any two of the circuit blocks, and said wiring line is formed in any layer of the semiconductor device;

(ii) planar-arranging the measurement terminals and the circuit blocks based on the design rules; and

(iii) establishing connection of each wiring line, which extends from one of the circuit blocks, via one of the measurement terminals.

Patentability of the Claims Under 35 U.S.C. §102(b)

The Examiner contends (see pg. 4 of the Office Action) that:

> The elements of the claims are summarized in col. 2, lines 16-52 [of *Dahl*], wherein planar-arrangement corresponds to the laying out of the bumps/bond pads, I/O cells, and edge logic cells in respective bumps/bond pads areas, I/O cell areas, and/or edge logic cell areas, wherein at least the edge logic cells correspond to the circuit blocks to be arranged, wherein bumps/bond pads and/or I/O cells correspond to the circuit blocks to be arranged, which include measurement terminals (i.e., JTAG terminals which are known in the art as terminals used for testing and/or measuring embedded integrated circuits) (see col. 17, lines 46-54; col. 15, lines 22-40); ...wherein the terminal/pad having electrode formed in an uppermost layer of the semiconductor device is further described in col. 7, lines 32-41....

With respect to the foregoing statement, the following is noted. *Dahl* (col. 16, lines 16-44) teaches a method of generating a padring design for a chip design including

(i) defining one or more styles for the padring layout design, wherein each style comprises one or more zones that each represent a portion of the padring design (see col. 16, lines 16-20);

(ii) defining one or more patterns for the one or more zones, wherein each pattern represents a template for one or more slots each comprising one or more areas (see col. 17-26); and

(iii) using each pattern in a process to create the slots in a respective zone, in a manner such that each area of each slot is associated with a particular location in the respective zone (see col. 16, lines 42-44).

That is, *Dahl* teaches a system in which a template pattern is provided for showing the position of each "area", i.e., a minimum area, in a relevant zone so as to automatically create a slot including the relevant area in the relevant zone which is a divided portion of the padring layout. Since various kinds of slots are possible, and assuming *arguendo* that a slot may be provided for measurement or testing, i.e., based on JTAG in the manner suggested by the Examiner, *Dahl* (e.g., col. 16, line 25-26), then *Dahl* arguably teaches that an area for measurement is also designed during an automatic layout design.

However, the present claimed invention includes measurement terminals, each having an electrode formed in an uppermost layer of the semiconductor device, and each being connectable to a wiring line for connecting any two circuit blocks, with the wiring line being formed in any layer of the semiconductor device, and the circuit blocks are automatically designed. *Dahl* fails to teach this aspect of the claimed invention.

Dahl (col. 7, lines 33-34) states that "the bump 400A is the metal that electrically couples the die to the package". In particular, *Dahl* (col. 7, lines 35-37) teaches that a solder ball is typically melted between the bump 400A and the package substrate. *Dahl* (col. 7, lines 37-34) also teaches that the solder ball may not be a ball but a cylinder created by the last few layers of the fabrication process. However, *Dahl* fails to teach that (i) each bump is a measurement terminal or that (ii) each bump is a measurement terminal that is connectable to a wiring line for connecting

any two of the circuit blocks, wherein the wiring line is formed in any layer of the semiconductor device, as recited in amended claims 1 and 5. The device in *Dahl* uses the bumps/pads to electrically couple the die to the package substrate.

Dahl (col. 7, lines 39-40) states: "Generally, the bump 400A is on the highest layer of metal (e.g., m7)". By using the word "generally" in this context, *Dahl* makes it clear that having a bump/pad in the uppermost layer of the semiconductor device is not essential, which is in sharp contrast to the present claimed invention.

In view of the foregoing, Applicants respectfully assert that *Dahl* fails to anticipate independent claims 1 and 5. Therefore, reconsideration and withdrawal of the rejection under 35 U.S.C. §102 are in order, and a notice to that effect is earnestly solicited.

Moreover, due to the fundamental above-discussed differences between the present claimed invention and *Dahl*, it is clear that the present invention is patentable over this reference under 35 U.S.C. §103.

Dependent Claims

In view of the patentability of independent claim 1, for the reasons set forth above, dependent claim 2 is patentable therewith over the prior art. In addition, this claim includes features which serve to even more clearly distinguish the present invention over the prior art.

Conclusion

Based on all of the above, it is respectfully submitted that the present application is now in proper condition for allowance. Prompt and favorable action to this effect and early passing of this application to issue are respectfully solicited.

Should the Examiner have any comments, questions, suggestions or objections, the Examiner is respectfully requested to telephone the undersigned in order to facilitate reaching a resolution of any outstanding issues.

It is believed that no fees or charges are required at this time in connection with the present application. However, if any fees or charges are required at this time, they may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,

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